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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/916,509	07/30/2001	Katsuhiko Hieda	04329.2613	8843

22852 7590 09/23/2005

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EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 09/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H'A

Office Action Summary	Application No.	Applicant(s)	
	09/916,509	HIEDA, KATSUHIKO	
	Examiner	Art Unit	
	Thao X. Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-21,24-44 and 48* is/are pending in the application.

4a) Of the above claim(s) *3-21 and 24-34* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *35-44,48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 04 Aug. 2005 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 35-44 and 48 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Recited 'the first conductivity type directly on the semiconductor substrate' limitation in claim 48 was not discloses in the original specification.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 35, 37-39, 44 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5115289 to Hisamoto et al.

Regarding claim 48, Hisamoto discloses a semiconductor device in fig. 3b comprising a semiconductor substrate 10 of first conductivity, column 12 line 63, a convex semiconductor layer 100, fig. 3b, of the first conductivity type, column 12 line 63, directly on the substrate 10, fig. 3b, a source and a drain region 40/50, column 6 line 41, provided on the substrate 10 and in the convex semiconductor layer 100, fig. 3b column 10 lines 51-54, a gate insulator 91, column 8 line 24, on the side surface of the convex semiconductor layer 100 and a top surface of the convex semiconductor layer 100, fig. 3b, a gate electrode 30, column 10 line 51, on a portion of the gate insulator 91 between the source and drain regions 40/50.

But, Hisamoto does not disclose a trench capacitor in the semiconductor substrate the trench capacitor 41 connected to one of source and drain

However, Hisamoto discloses a trench capacitor 41, fig. 5 column 11 line 54, in the semiconductor substrate, fig. 5, and the trench capacitor 41 connected to one of source and drain, fig. 5. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the trench capacitor

teaching of Hisamoto in fig. 5 to create a memory structure in conjunction with fig. 3B, because such memory structure is typical in the art, see also fig. 25C.

Regarding claim 35, Hisamoto discloses a semiconductor device wherein a distance between the S/D 40/50 regions becomes longer toward a lower portion from the upper portion of the convex semiconductor layer 100, fig. 4e.

Regarding claim 37, Hisamoto discloses a semiconductor device wherein the sidewall gate portion 30 is formed to portion under the S/D region 40/50, fig. 1 along the side surface of the convex semiconductor layer 100, fig. 1.

Regarding claim 38, Hisamoto discloses a semiconductor device wherein a width of the convex semiconductor layer is smaller than 0.2 μm, column 7 lines 35-55.

Regarding claim 39, Hisamoto discloses a semiconductor device wherein a width of the convex semiconductor layer 100 is smaller than the depth of the S/D region 40/50, fig. 1.

Regarding claims 44, Hisamoto discloses a semiconductor device wherein a position of a deepest portion of the gate electrode is deeper that a position of the deepest portion of the S/D region, fig. 1.

6. Claims 36 and 40-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5115289 to Hisamoto et al in view of US 6316813 to Ohmi et al.

Regarding claim 36, Hisamoto does not disclose a semiconductor device wherein the impurity concentration of the S/D region 40/50 becomes lower toward a lower portion from an upper portion of the convex semiconductor layer.

However, Ohmi discloses a semiconductor device wherein the impurity concentration of the S/D region 40/50 becomes lower toward a lower portion from an upper portion of the convex semiconductor layer, fig. 8D. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the doping teaching of Ohmi with Hisamoto, because it would have created a LDD structure.

Regarding claims 40-42, Hisamoto discloses a semiconductor device wherein at least one of the S/D regions 40/50 and the convex semiconductor 100 is electrically connected to the conductive substrate, fig 5.

But Hisamoto does not disclose a semiconductor device wherein at least one of the S/D regions includes at least two kinds of diffusion layers, a high and low concentration, having a dense impurity concentration diffusion layer.

However, Ohmi discloses a semiconductor device wherein at least one of the S/D regions 40/50 includes at least two kinds of diffusion layers 6 and 37, a high and low concentration N^+ and N^-, having a dense impurity concentration diffusion layer, and the convex semiconductor is electrically connected to the conductive substrate, fig 8D. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the doping teaching of Ohmi with Hisamoto, because it would have created a LDD structure.

7. Claims 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 5115289 to Hisamoto et al in view in view of US 6333229 to Furukawa et al.

Regarding claims 43, Hisamoto discloses a semiconductor device comprising a gate insulating film 91 is made of a silicon oxide, column 8, line 30.

But Hisamoto does not disclose the gate oxide comprises the oxide including at least one of Ta, Ti.

However, Furukawa reference disclose the gate oxide layer 30 comprise silicon oxide, titanium oxide, and tantalum oxide, column 3 lines 48-52. At the time of the invention was made; it would have been obvious to one of ordinary skill in the art to replace the gate silicon oxide of Ohmi with titanium or tantalum oxide gate oxide teaching of Furukawa, because such material substitution would have been considered a mere substitution of art-recognized equivalent material.

8. Claim 48 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 4979014 to Hieda et al. in view of US 5115289 to Hisamoto et al.

Regarding claim 48, Hieda discloses a semiconductor device in fig. 1F comprising a semiconductor substrate 10 of first conductivity (P), fig. 1F, a convex semiconductor layer 10a, fig. 1F, of the first conductivity type (P) directly on the substrate 10, fig. 1F, a source and a drain region 19/20, fig. 1F, provided on the substrate 10 and in the convex semiconductor layer 10a, a gate insulator 17, column 3 line 7, on the side surface of the convex semiconductor layer 10a and a top surface of the convex semiconductor layer 10a, fig. 1G, a gate electrode 18, column 3 lines 9 and 14, on a portion of the gate insulator 17 between the source and drain regions 19/20.

But, Hieda does not disclose a trench capacitor in the semiconductor substrate the trench capacitor 41 connected to one of source and drain.

However, Hisamoto discloses a trench capacitor 41, fig. 5 column 11 line 54, in the semiconductor substrate 60', fig. 5, the trench capacitor 41 connected to one of source and drain, fig. 5. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the trench capacitor teaching of Hisamoto in Hieda's device, because such memory structure is typical in the art.

Response to Arguments

9. Applicant's arguments with respect to claims 35-44 and 48 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao X. Le
20 Aug. 2005

Trench Isolated (TIS) Transistor (1987 IEDM)

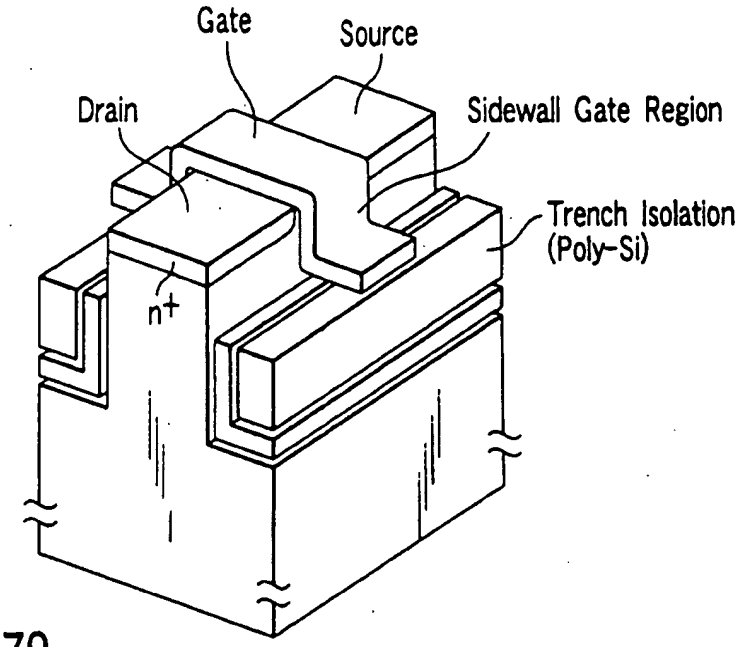


FIG. 79 Prior Art

OK
TL
9/16/05

DELTA STRUCTURE (1989 IEDM)

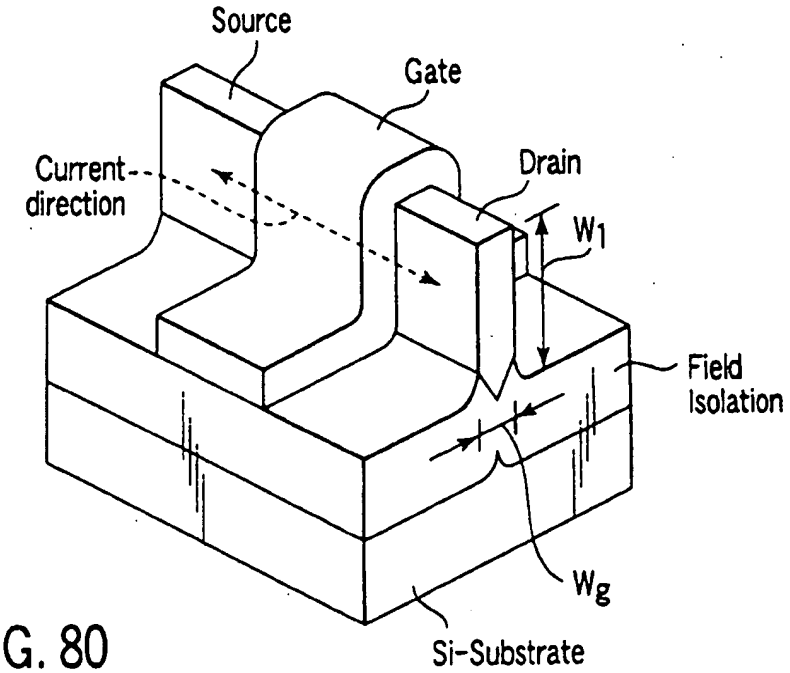
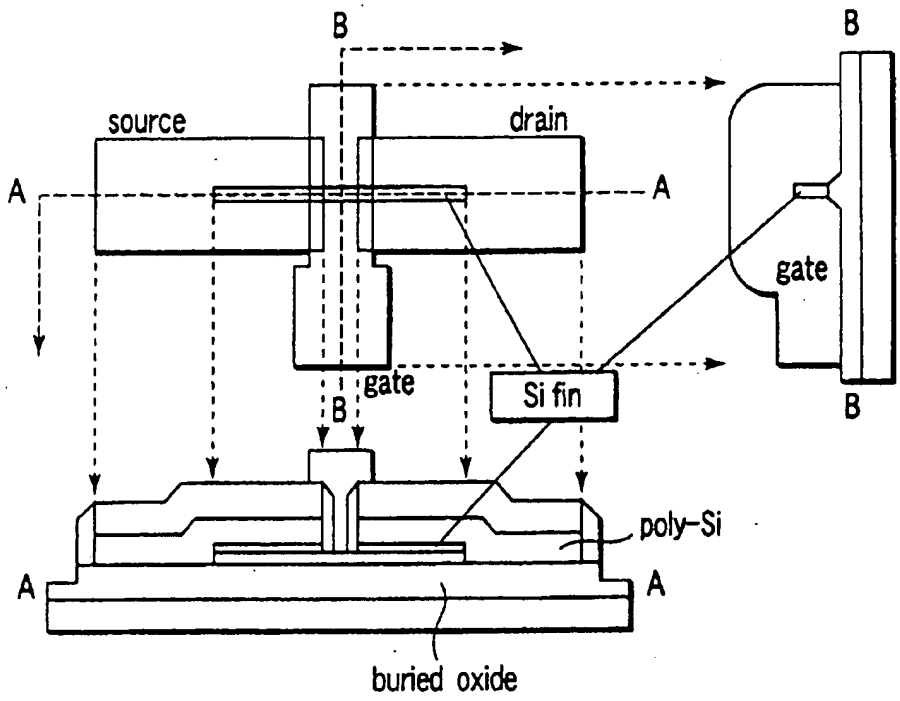


FIG. 80 Prior Art

Replacement Sheet

Folded-channel MOSFFT (1998 IEDM)



Prior Art

FIG. 81

OK
TZ
9/16/05